Design for time interleaving of data using sub-sampling clocks

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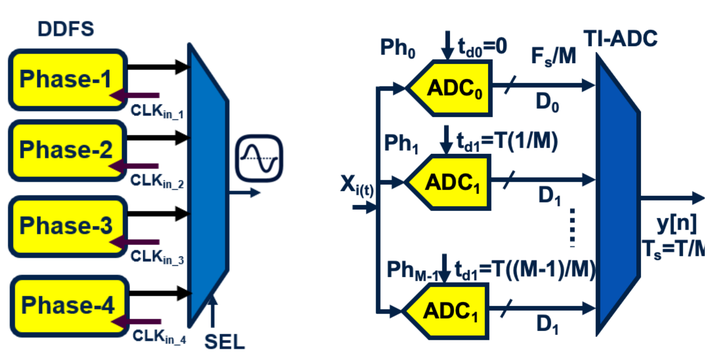
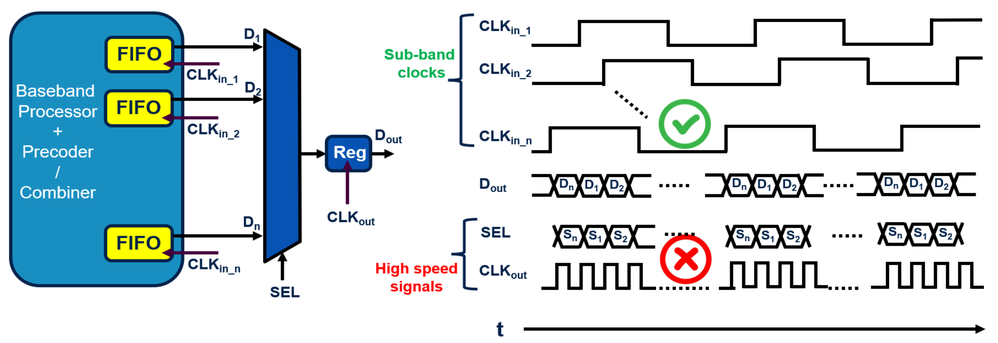


MOTIVATION

HF time interleaving of data

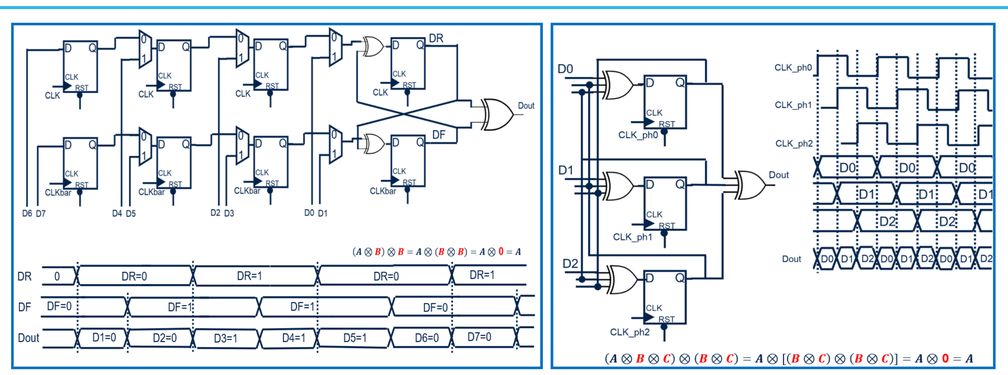
- Using slow clocks
- Glitch-free operation
- No clock signal in datapath
- Relaxed timing
- Low-power operation
- Independent technology



PROBLEM

Remove HF signals

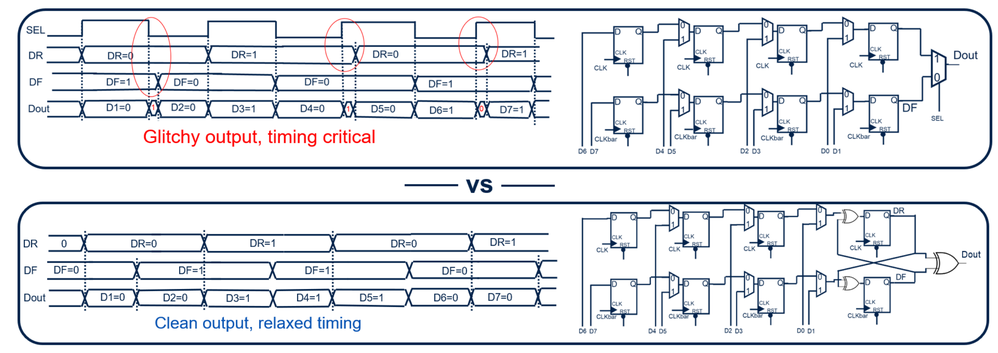
- Time interleaving LF input data Dn
- Remove D_{out} output MUX
- D_{out} at fast-rate without using SEL and fast clock CLK_{out}
- Devise a mechanism for sub-band clocks CLK_{in_n} to generate full-rate output D_{out}



SOLUTION

Full rate at slow clock

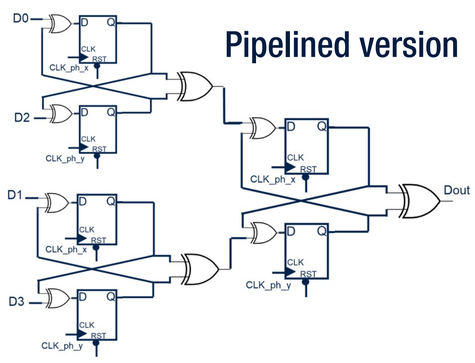
- Final stage MUX “selection” & “fast clock” eliminated
- Grey logic terminal XOR ensures glitch-free operation
- Demonstrated for double data rate & interleave by 3



EVIDENCE

Prior vs proposed

- Final stage MUX “selection” has high timing sensitivity and can cause glitch at D_{out}
- Glitch possibility eliminated for D_{out} as only one signal (DF or DR) changes at any clock edge



CONCLUSION & NEXT STEPS

- A new design for interleaving N data with using input clocks is proposed
- Grey signaling at the output ensures glitch-free, robust operation with relaxed timing
- Scalable to any number of input data
- Pipelined, modular architecture realizations suited across applications
- Sub-band clock interleaving saves power and simplifies design
- The design is technology independent and resilient to PVT variations